HIGH POWER CONTROL COMPONENTS USING A NEW MONOLITHIC FET STRUCTURE

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ABSTRACT

A new monolithic switch FET (MFET)* control device has been developed that can be integrated with other monolithic functions or used as a discrete component in a MMIC structure. This device increases the power handling capability of the conventional switch FET (SFET) by an order of magnitude. It does this by overcoming the breakdown voltage limitation of the SFET device. The design, fabrication, and performance of two high power control components using MFET devices are described as examples of the implementation of this technology (an L-Band terminated single pole single throw (SPST) switch, and an L-Band limiter).

INTRODUCTION

This paper summarizes the beneficial use of GaAs MMIC technology in high power (10 to 100 W range) signal control applications. The microwave signal switching component which is still in common use today is the silicon PIN diode. However, the GaAs switch FET is finding quick acceptance as a PIN diode replacement in several applications, the advantages being fast switching speeds, simplified bias networks, monolithic compatibility, and lower power consumption driver circuitry. GaAs switch FET technology has been demonstrated over wide bandwidths at low power levels (20 dBm) [1]. Higher power levels have been attained by using impedance transformation; this technique places the switch FET at a lower impedance point and thus reduces the voltage stress on the device. Ten Watt switches have been demonstrated with this technique by transforming from 50 to 18 ohms [2]; however, due to the required impedance transformation, the approach is applicable over limited frequency bandwidth. The MFET device discussed in this paper is a suitable replacement for PIN diodes as a generic control element in applications from ten Watts to several hundred Watts CW, and has all the advantages of the GaAs switch FET (in comparison to the PIN diode). Two control functions implemented with this new device are presented as examples of its utility as a high power PIN diode replacement.

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MFET DEVICE DESCRIPTION

The power performance of an SFET is limited by its current handling capability in its low impedance state, and by its breakdown voltage in its high impedance state. The current handling of an SFET can be increased by increasing its periphery. The maximum peak voltage that an SFET can control, on the other hand, is given by:

$$V_{max} = VB - VP$$

where VB is the device breakdown voltage and VP is the pinchoff voltage. V_{max} ranges between 10 and 18 volts for most GaAs foundries. This corresponds to a range of 1 to 3.25 Watts in a 50 Ohm system. PIN diodes have breakdown voltages five to ten times higher then SFETs and can, therefore, control much higher voltages. Thus, to achieve the benefits of GaAs switch FET technology at high power levels a new approach that is capable of controlling larger voltage swings is required. The MFET device structure has been developed to meet this requirement.

The MFET is composed of several FET cells connected in series so that the voltage across the MFET is evenly divided among these cells. The FET cell is a three terminal device and it is important to balance both the DC and RF voltages evenly across the three terminals of each

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cell of the MFET both in the steady state and during switching transients. The MFET designed in this fashion multiplies the peak voltage control capability of the SFET by N, where N is the number of FET cells connected in series. Thus the MFET power handling capability is N^2 times higher than that of the SFET. For example, in a 50 ohm system, an SFET with an 18 volt V_{max} can control 3.25 Watts, where as a four cell MFET device can control 50 Watts.

Figure 1 shows an example of an MFET made up of three cells. As can be seen

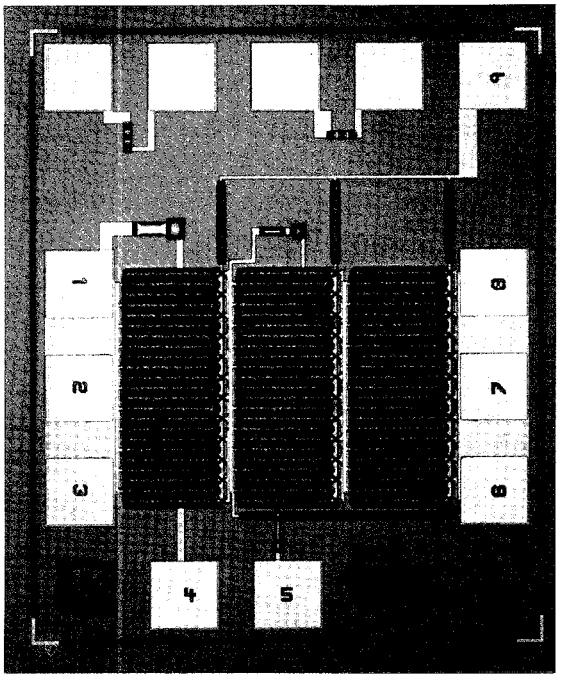

Figure 1. Photograph of a three cell MFET switching device.

various passive elements are required to balance all the voltages. The schematic of this chip is provided in Figure 2. The core of the MFET design is the three series connected FETs. The FETs share a common periphery W. This periphery is determined by the peak current the MFET must control. The number of series connected FETs is determined by the peak RF voltage swing that the MFET must control. Additional elements are incorporated in the MFET design to achieve an even voltage distribution across the FETs in the MFET. For example, the MFETs were used mounted in a microstrip hybrid. In this configuration, the FETs in the MFET have a parasitic capacitance to the ground plane through the chip. This parasitic causes a nonuniform voltage distribution across the FETs in the series stack. The

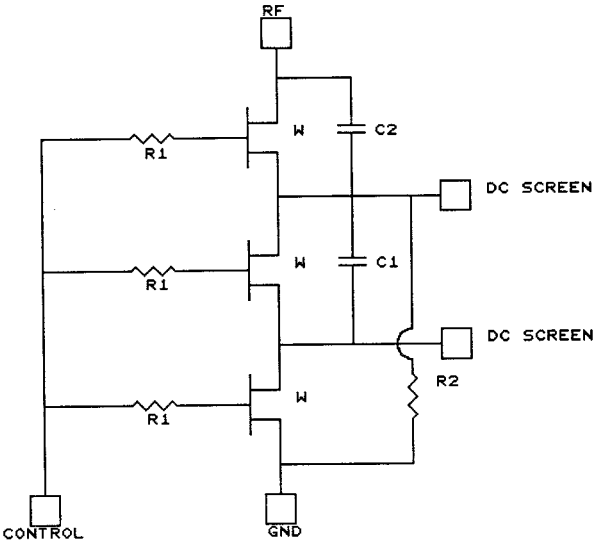

Figure 2. This is a schematic of the MFET chip shown in Figure 1.

two capacitors in the schematic of Figure 2 have been added to compensate for this effect. For a stack of N FETs there are N-1 capacitors and their values can be determined by the following equation:

$$Ci = i(i-1)Cp/2$$

where Cp is the parasitic capacitance, and Ci is the compensation capacitor connected across the ith FET from the ground end of the stack. There are several options for bias networks. For this MFET a resistive bias network was selected. The value of the R1 resistors in Figure 2 must be 40 to 80 times larger than the impedance of the gate capacitance at the minimum frequency of operation. By making these resistors approximately equal in value, all the FETs will turn ON or OFF simultaneously so that an even RF voltage distribution is maintained across them during switching transients. The demonstration device shown in Figure 1 has been tested to 27 Watts corresponding to 52 volts peak RF voltage, in a 50 ohm system. However, the device did show signs of insertion loss compression at 21 Watts. This corresponds to 45 volts. Thus, each FET cell in this particular process is capable of controlling 15 volts.

A four cell MFET device has also been fabricated. Based on the three cell results, its power control capability in 50 ohms is expected to be 40 Watts. This device was tested up to 27 Watts with no sign of compression.

These devices are used in the same fashion as an SFET with gate bias resistors already integrated. Both of these MFETs have been used in the fabrication of the control functions described in this paper.

L-BAND TERMINATED SPST

This SPST switch is designed to operate at 1.5 GHz with an octave bandwidth. The SPST is an all shunt design as shown in the schematic in Figure 3. The switch

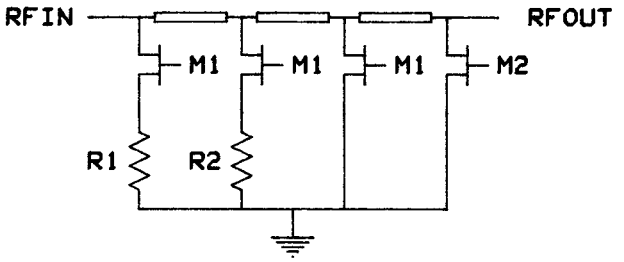

Figure 3. Circuit topology used for the matched SPST switch.

has an asymmetric design in that there is a high (RFIN) and low (RFOUT) power port. The RFOUT port is shunted by an MFET designated M_2. This MFET is sized to provide a low power match to the output when the switch is in the isolation state. The MFETs labeled M_1 are much larger in periphery since they must cope with a higher current level than M_2. This switch is an absorptive switch and therefore, must dissipate the incident RF power when the switch is in the isolation state. The resistors labeled R_1 and R_2 are high power chip resistors sized to handle the RF power dissipation. Their values were designed to provide a good match over the band, and balance the current evenly between the M_1 elements. The switch was fabricated using microstrip transmission lines as shown in Figure 4.

Figure 5 shows the measured insertion loss and isolation on a 40 Watt version of the terminated switch topology. This switch was fabricated with four-cell MFETs. The insertion loss is a maximum of .75 dB across the band, and the isolation is a minimum of 24 dB. The simulations of insertion loss and isolation fit to within .1 and 1 dB respectively. Figure 6 shows the switch return loss at both ports in both states.

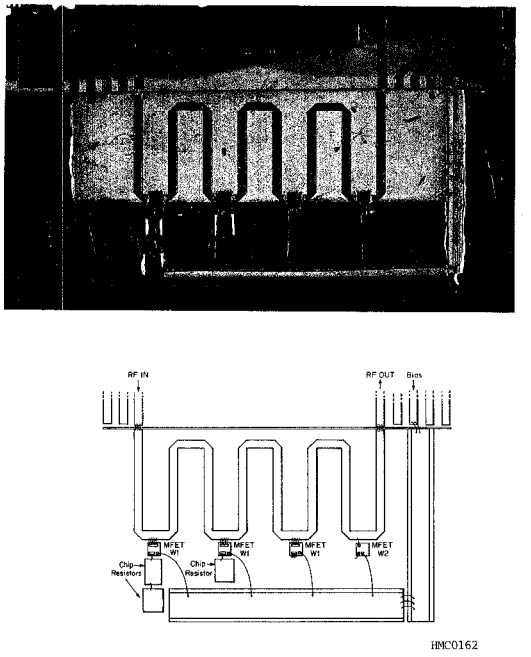

Figure 4. Picture and drawing of a terminated high power SPST switch.

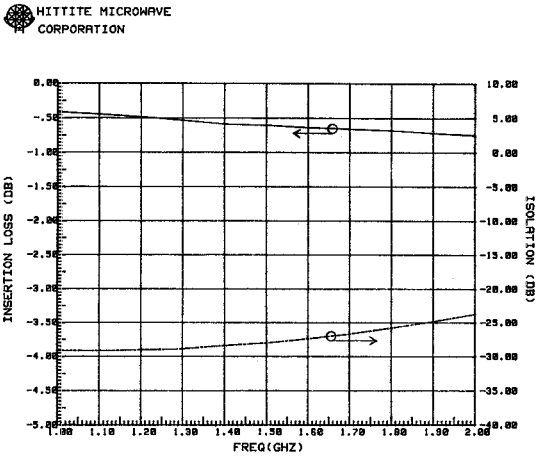

Figure 5. Measured insertion loss and isolation of a matched SPST switch, fabricated with four cell MFET devices.

The return loss at both ports was equal or better than 15 dB across the band in the transmission state. For the isolation state, the output return loss decreased to 9 dB at 1 GHz.

Figures 7 and 8 show the power performance of this SPST fabricated with four-cell MFETs. The switch was tested, and did not expand (out of isolation) or compress (out of insertion loss) up to 27 Watts (the limit of the TWTA that was available for measurements).

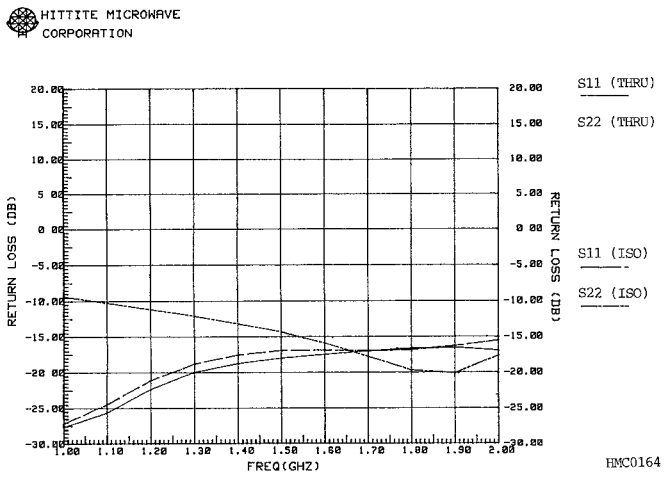

Figure 6. Measured return loss performance of a SPST switch in both states, fabricated with four cell MFETs.

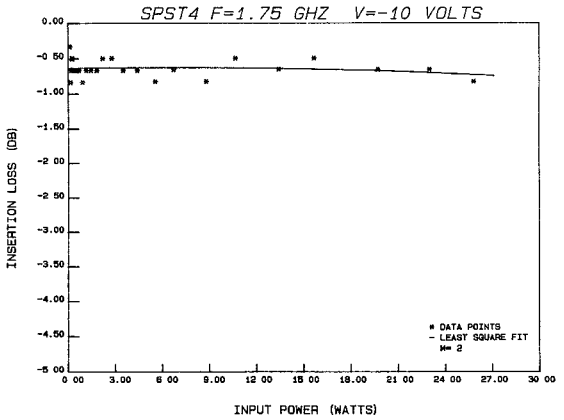

Figure 7. Measured insertion loss vs. input power for a SPST switch fabricated with four-cell MFETs.

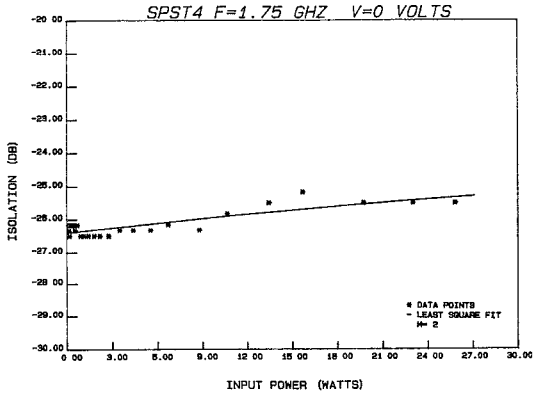

Figure 8. Measured isolation vs. input power for a SPST switch fabricated with four-cell MFETs.

Figures 9 and 10 show the power performance of another version of the SPST, which was fabricated with three cell MFETs. For a 0 to 21 Watt input power level range, the isolation expands by less then 1 dB and the insertion loss compresses by less then 1 dB. Thus, the three cell MFET can control up to 20 Watts in a 50 ohm system. This corresponds to 45 volts or 15 volts per cell.

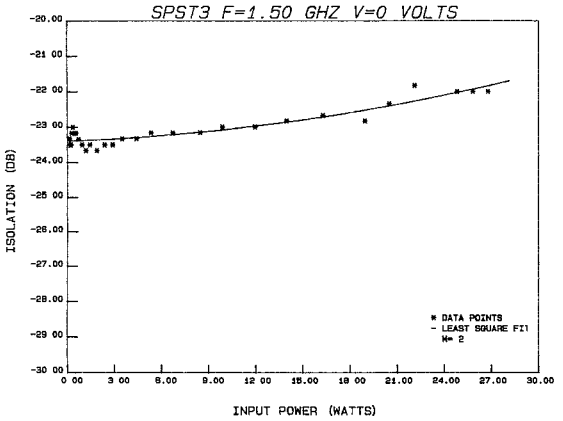

Figure 9. Measured isolation vs. input power for a SPST switch fabricated with three cell MFETs.

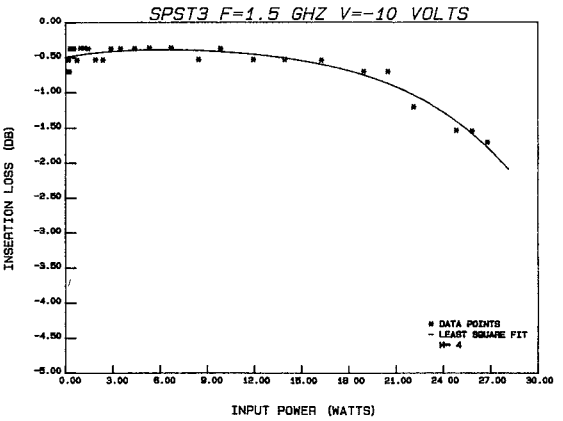

Figure 10. Measured insertion loss vs. input power for a SPST switch fabricated with three cell MFETs.

L-BAND LIMITER

The block diagram of the limiter is shown in Figure 11. The limiter is composed of two components; a Voltage Controlled Attenuator (VCA) and Voltage Multiplier (VM) amplitude detector circuit. In operation the VM detects the RF amplitude of the output of this

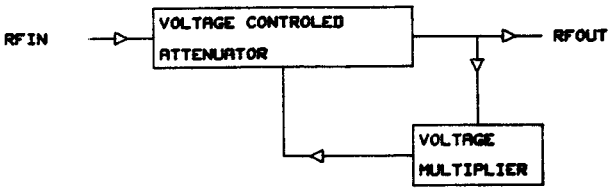

Figure 11. Block diagram for the limiter.

attenuator. The DC voltage of the output of the VM is fed back to the control input of the attenuator. The VM output voltage acts to increase the attenuation level as the RF input level increases. A fixed DC bias is superimposed on the output of the detector to adjust the limiting threshold.

The SPST switch described in the previous section was designed to provide low return loss even at intermediate gate control voltages between transmission and isolation. It is thus ideally suited for use as a voltage controlled attenuator.

A doubler circuit was used for the voltage multiplier. Figure 12 shows a picture of the voltage doubler chip. However, it was found that diode parasitics and output loading reduced the output voltage from this circuit to only 40% of the peak RF voltage on its input. Hence, it was necessary to include an operational amplifier between the detector circuit on the attenuator control input so as to provide enough loop gain. Figure 13 shows the measured performance of this limiter configuration, at two different DC offset bias settings.

CONCLUSION

GaAs MMIC technology is generally considered to be applicable for small to medium power levels in the 1 to 2 Watt range. This paper summarizes the successful implementation of this technology in power control components at an order of magnitude higher power levels by demonstrating the concept of a GaAs monolithic power control device. Two examples of its integration into power control functions have been presented.

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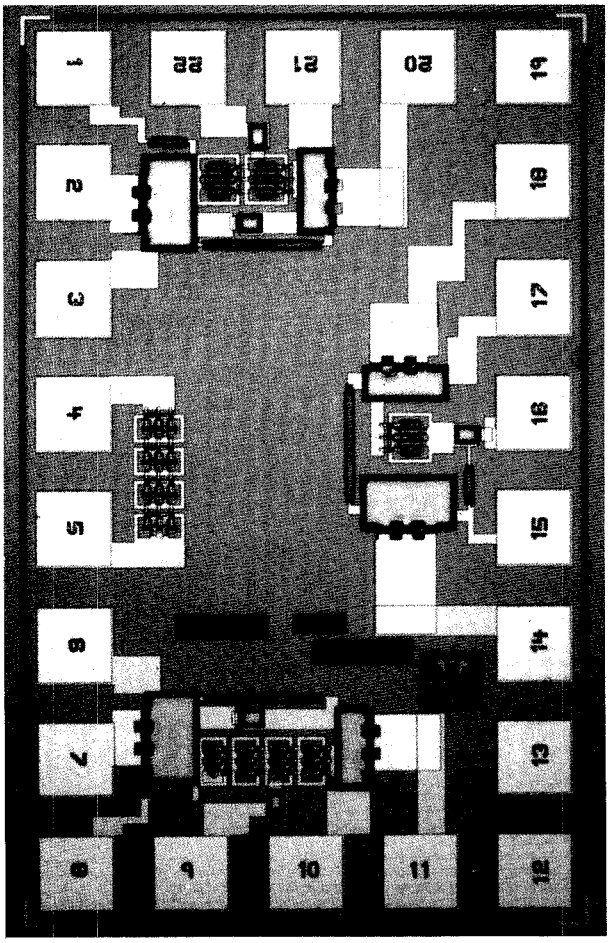

Figure 12. Voltage-multiplier detector MMIC chip.

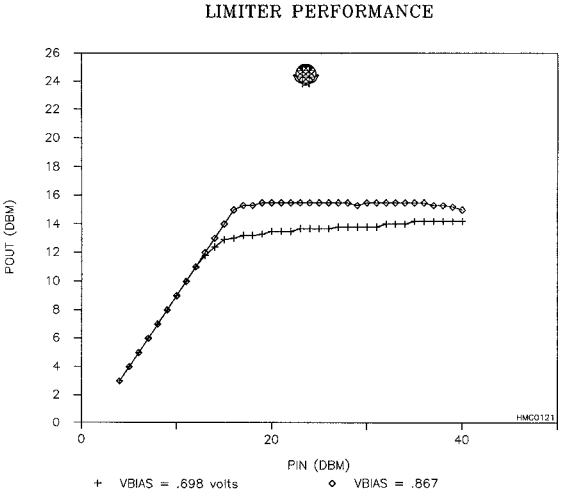

Figure 13. Measured performance of the limiter outlined in Figure 11.

REFERENCES

[1] M.J. Schindler, A.M. Morris, "DC-40 GHz and 20 - 40 GHz MMIC SPDT Switches", IEEE Microwave and Millimeter Wave Circuits Symposium, 1987, pp. 85-88.

[2] Y. Ayasli, R. Mozzi, L. Hanes, L.D. Reynolds, "An X-Band 10 W Monolithic Transmit-Receive GaAs FET Switch", IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, May 1982, pp. 42 - 46.